ABSTRACT OF THE DISCLOSURE

In a system for encoding, transmitting, and decoding data in real time, synchronization is established between encoder end decoder ends with ease and reliability no matter if jittering occurs in a transmission path and no matter what encoding bit rate is used. A change of a difference d between STC (output value of STC counter) at the decoder end and SCR extracted from an encoding stream (MPEG2-PS) is integrated over a given time. Depending on whether the integrated value is positive or negative, a determination is made whether the data processing speed at the decoder end is faster than the encoder end. When the integrated value is positive, the input clock frequency of the STC counter at the decoder end is reduced, and when the integrated value is negative, the input clock frequency thereof is increased. Alternatively, when the integrated value is positive, the input clock frequency of the STC counter at the encoder end may be increased, and when the integrated value is negative, the input clock frequency thereof may be reduced.